REMARKS

Claims 1 - 11 are pending in the present application, wherein claims 10 and 11 are newly added. Applicants are requesting reconsideration of the present application.

Applicants are amending claim 7 to properly introduce an element, and amending claim 9 to avoid use of "and/or." Neither of these amendments narrows the meaning of any term of the claims, and therefore, the doctrine of equivalents should be available for all of the elements of all of the claims.

On page 2 of the Office Action, claims 1 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,324,664 to Farwell et al. (hereinafter "the Farwell et al. patent") in view of U.S. Patent No. 6,055,285 to Alston (hereinafter "the Alston patent"). Applicants are traversing this rejection.

Claim 1 provides for a testing unit for testing a device under test (DUT). The testing unit includes, *inter alia*, a synchronizing unit that receives a first clock signal from the DUT and a second clock signal from the testing unit. The synchronizing unit includes (a) a buffer for buffering data, (b) a write unit for writing data from the DUT into the buffer, wherein the first clock signal controls a write access onto the buffer, and (c) a read unit for reading out data from the buffer to be provided to a receiving unit, wherein the second clock signal controls a read access onto the buffer.

The Office Action, on page 3, recognizes that the Farwell et al. patent does not specifically disclose that a first clock signal controls a write access into a buffer, and a second clock signal controls a read access onto the buffer. Therefore, the Office Action introduces the Alston patent, and states that it would have been obvious to supplement the apparatus disclosed by the Farwell et al. patent with the synchronization circuit disclosed by the Alston patent. The Office Action further indicates that the suggestion/motivation for combining the Farwell et al. and Alston patents would have been to synchronize the transfer of data. Applicants respectfully disagree with the Examiner's assessment of the Farwell et al. and Alston patents.

The Farwell et al. patent, with reference to FIG. 1, discloses an integrated circuit 10 coupled to external test equipment 33 via a test bus 31. Integrated circuit 10 includes combinatorial logic 15, a scan path 20, an output memory 25, a modulo counter 27, a read/write controller 19, and a test bus controller 29.

In the Farwell et al. patent, it is readily apparent that integrated circuit 10 is a device under test. Thus, test bus 31 is an interface between a device under test, i.e., integrated circuit 10, and external test equipment 33. To the extent that the Farwell et al. patent is similar to the testing unit of claim 1, it is at test bus 31 where the testing unit of claim 1 would be applied for synchronizing a data stream between integrated circuit 10 and external test equipment 33. However, the Farwell et al. patent does not describe any kind of problem being encountered at test bus 31, and therefore does not disclose any motive to modify test bus 31. Since the Farwell et al. patent does not describe any kind of problem being encountered at test bus 31, **a person would not would not be prompted to modify the arrangement thereof** on the basis of the disclosure of the Alston patent, or any other reference, to produce the testing unit of claim 1.

Nevertheless, the system in the Farwell et al. patent employs a system clock (SYSCLK) and accommodates a test clock (TEST CLOCK) that may be asynchronous relative to the system clock (col. 5, lines 33 - 38). More specifically, the system in the Farwell et al. patent accommodates this potential asynchronous relationship by utilizing modulo counter 27 to provide an index that enables output memory 25 to sample the output of scan path 20 (col. 4, lines 39 – 42), i.e., to write data into output memory 25, and by utilizing test bus controller 29[1] to read output memory 25 (col. 4, lines 44 – 45).

Whereas the Farwell et al. patent expressly states that the system accommodates asynchronous clocks, there is no apparent need to modify the Farwell et al. patent to include the synchronization circuit of the Alston patent. Moreover, if the Farwell et al. patent were modified to include the

[1] The Farwell et al. patent, at col. 4, line 44, refers to "test bus controller 27", but from FIG.1, it is clear that the Farwell et al. patent intended to refer to "test bus controller 29."

synchronization circuit of the Alston patent, such a modification would obviate the manner in which modulo counter 27 and test bus controller 29 coordinate the writing of data to, and reading of data from, output memory 25, thus changing the principle of operation of the Farwell et al. patent. Hence, the cited combination of the Farwell et al. and Alston patent is **improper for purposes of a section 103(a) rejection** of claim 1.

Below, Applicants further elaborate on the reasons as to why the cited combination of the cited references is improper for purposes of the rejection.

The Farwell et al. patent concerns a test circuit for an integrated circuit device, and the preferred embodiment of test circuit is shown in FIG. 1. The Farwell et al. patent concerns the field of circuit testing in which digital circuits having built-in test circuits are considered, namely test circuits using a scan chain. The functionality of such a scan chain is well known in the art. As is specified in the introductory portion of the Farwell et al. patent, a problem with such approaches is that the entire arrangement is operated on the basis of an external test clock frequency which might be different and/or asynchronous relative to a system clock frequency at which the device under test, under normal operation, performs its operational functions. This might result in the undesirable situation that such testing is not available for integrated circuits including dynamic logic, as such dynamic logic requires a continuous refresh which is not provided due to the use of the external test clock, as it is outlined in col. 1, lines 44 to 52 of the Farwell et al. patent.

To overcome this problem, the Farwell et al. patent teaches an approach in which an external test clock, i.e., TEST CLOCK, as well as a system clock, i.e., SYSCLK, are used, wherein the test clock TEST CLOCK is used for exchanging data between the device under test and the external test equipment, and wherein the system clock SYSCLK is used for operating the internal structure of the integrated circuit, namely the scan chain as well as the circuitry to be tested. The basic functionality of the device shown in FIG. 1 of the Farwell et al. patent is that, for testing, respective bits are serially input into flip flops (i.e., S(0) through S(Y-1)) of the scan chain via an input memory 18 under control of the test clock TEST CLOCK. Then the system clock SYSCLK is used to operate scan path 20 and

combinatorial logic 15 to obtain desired output signals from combinatorial logic 15 which are, again, stored in scan path 20. The system clock SYSCLK is continuously applied to combinatorial logic 15 and scan path 20, so that in combinatorial logic 15, dynamic logic elements can be used as a continued refresh is provided, and further, the signals stored in scan path 20 are "circulated" via a feedback path from the output of scan path 20 back to the input of a multiplexer 17.

While this solves the problem concerning the use of dynamic logic elements in integrated circuit 10, it must now be ensured that upon reading out the test results, the proper sequence of bits stored in scan path 20 is also read out via output memory 25. Therefore, in accordance with the teachings of the Farwell et al. patent, modulo counter 27 indicates to read/write controller 19 which bit is currently present at the output of scan path 20, as described with regard to the table shown in col. 5 of the Farwell et al. patent. Since the read out starts with the first bit originally held in flip flop S(0), the read out of the data will start when modulo counter 27 indicates that this bit is present at the output of scan path 20, and then, via read/write controller 19, an enable signal to output memory 25 is provided for allowing a write access to output memory 25 to store the bit. Then, under control of the test clock TEST CLOCK, output memory 25 is read out, and the data therefrom is forwarded to external test equipment 33 (see col. 4, line 25 to col. 5, line 4).

Thus, the basic functionality of the system in the Farwell et al. patent is such that the internal circuitry and the test equipment are operated by different clocks which, in turn, requires some manner of synchronization. This is achieved by signaling to read/write controller 19 which bit is currently present at the output scan path 20. Since read/write controller 19 receives the test clock TEST CLOCK but not the system clock SYSCLK, the write access and the read access to output memory 25 are controlled by the same clock signal, namely the test clock TEST CLOCK.

Thus, the Farwell et al. patent provides for data synchronization, and so, there is no suggestion or motivation in the Farwell et al. patent to modify the functionality therein to include the synchronization circuit of the Alston patent. Moreover, as the Farwell et al. patent already accommodates asynchronous clocks such a modification, an incorporation of the synchronization circuit of the Alston patent would

provide no apparent improvement of the system in the Farwell et al. patent. Moreover, incorporating the synchronizing circuit of the Alston patent into the test system of the Farwell et al. patent would require a redesign of the functionality of the Farwell et al. patent thus changing the principle of operation of the Farwell et al. patent. Accordingly, as mentioned above, the cited combination of the Farwell et al. and Alston patent is **improper for purposes of a section 103(a) rejection** of claim 1.

For the several reasons provided above, Applicants submit that claim 1 is patentable over the cited combination of the Farwell et al. and Alston patents.

Claims 2 – 7 depend from claim 1. At least because of this dependence, claims 2 – 7 are also patentable over the cited combination of the Farwell et al. and Alston patents. Nevertheless, below, Applicants are highlighting a further point of distinction of claims 6 and 7.

Claim 6 depends from claim 1, as mentioned above, and further recites that the buffer provides an initial delay time between a first valid write access and a first valid read access. The Farwell et al. patent does not suggest any need for such a modification of the functionality of output memory 25. Moreover, such a modification makes no sense as, in accordance to the present invention, the delay is selected to make sure that any overlap between the two accesses is avoided without the need for an additional control signal, whereas the Farwell et al. patent explicitly teaches the provision of such a control signal in the form of the scan index provided by modulo counter 27. Therefore, a person of ordinary skill would not consider modifying the circuitry of the Farwell et al. patent to achieve the functionality of claim 6, and, therefore would also not consider combining the disclosure of the Alston patent to achieve the functionality of claim 6. Accordingly, Applicants submit that claim 6, in addition to its benefiting from its dependence on claim 1, is further patentable over the cited combination of references, on its own merits.

Claim 7 depends from claim 6, and therefore, like claim 6, is also further patentable over the cited combination of references, on its own merits.

Claim 8 is an independent claim, and includes recitals similar to those of claim 1, as described above. Thus, claim 8, for reasoning similar to that provided in support of claim 1, is also patentable over the cited combination of the Farwell et al. and Alston patents.

Claim 9 depends from claim 8. By virtue of this dependence, claim 8 is also patentable over the cited combination of references.

Applicants respectfully request reconsideration and withdrawal of the section 103(a) rejection of claims 1 – 9.

Applicants are adding claims 10 and 11 to even further provide the claim coverage that Applicants appear to deserve based on the prior art that was cited by the Examiner. A favorable consideration that also results in the allowance of claims 10 and 11 is earnestly solicited.

In view of the foregoing, Applicants respectfully submit that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicants respectfully request favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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